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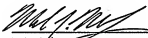
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in the following listed application(s) or patent(s) for which the issue fee has been paid.

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7,535,053 B2	10/694,477	May 19, 2009	October 27, 2003	4264	0553-0118.01

Respectfully Submitted,



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(12) **United States Patent**
Yamazaki

(10) **Patent No.:** US 7,535,053 B2
(45) **Date of Patent:** *May 19, 2009

(54) **NONVOLATILE MEMORY AND
ELECTRONIC APPARATUS**

- (75) Inventor: Shunpei Yamazaki, Tokyo (JP)
(73) Assignee: Semiconductor Energy Laboratory
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(*) Notice: Subject to any disclaimer, the term of this
patent is extended or adjusted under 35
U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

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Nov. 16, 1998, now Pat. No. 6,686,623.

(30) **Foreign Application Priority Data**

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Nov. 26, 1997 (JP) 9-340754

- (51) Int. Cl. **H01L 29/78** (2006.01)
(52) U.S. Cl. 257/316; 257/345
(58) Field of Classification Search 257/316,
257/345, 347, 349, 354

See application file for complete search history.

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(57) **ABSTRACT**

An active region, a source region, and a drain region are formed on a single crystal semiconductor substrate or a single crystal semiconductor thin film. Impurity regions called pinning regions are formed in striped form in the active region so as to reach both of the source region and the drain region. Regions interposed between the pinning regions serve as channel forming regions. A tunnel oxide film, a floating gate, a control gate, etc. are formed on the above structure. The impurity regions prevent a depletion layer from expanding from the source region toward the drain region.

45 Claims, 17 Drawing Sheets

